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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,447	10/30/2001	Siuki Chan	X-885 US	6106

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
BHAT, ADITYA S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,447	CHAN, SIUKI	
	Examiner	Art Unit	
	Aditya S Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9 and 19-26* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Honda et al. (USPN 5,497,109)

With regards to claim 1, Honda et al. (USPN 5,497,109) teaches a method of measuring signal skew of a signal tree on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, the method comprising:

a. instantiating a first delay element on the device using a first programming sequence that includes:
i. connecting the first destination branch to the input terminal of the first logic block; (Col. 1, lines 21-29) and
ii. connecting the output terminal of the first logic block to the input terminal of the second logic block; (Col. 1, lines 21-29) and
b. instantiating a second delay element on the device using a second programming sequence that includes:
i. connecting the third destination branch to the input terminal of the third logic block; (See figure 1) and
ii. connecting the output terminal of the third logic block to the input terminal of the second logic block.(See figure 1)

With regards to claim 2, Honda et al. (USPN 5,497,109) teaches that a signal tree is a clock tree.(Col. 1, lines 21-22)

With regards to claim 3, Honda et al. (USPN 5,497,109) teaches that the input terminal of the second logic block is an asynchronous input terminal. (See figure 8)

With regards to claim 4, Honda et al. (USPN 5,497,109) teaches that the first, second, and third logic blocks are arranged on the device in a column. (See figure 1)

With regards to claim 5, Honda et al. (USPN 5,497,109) teaches that the second, logic block is physically between the first and the third logic block. (see figure 1)

With regards to claim 6, Honda et al. (USPN 5,497,109) teaches that the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the logic blocks having an input terminal and an output terminal, the method further comprising:

c. instantiating a third delay element on the device using a third programming sequence that includes:

i. connecting the fourth destination branch to the input terminal of the fourth logic block; (See figure 1) and

ii. connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block; (See figure 1) and

d. instantiating a fourth delay element on the device using a fourth programming sequence that includes:

i. connecting the sixth destination branch to the input terminal of the sixth logic block; (See figure 1) and

ii. connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block. (See figure 1)

With regards to claim 8, Honda et al. (USPN 5,497,109) teaches that configuring the device to include the first and second delay elements in respective first and second oscillators. (311; See figure 2)

With regards to claim 9, Honda et al. (USPN 5,497,109) teaches that comparing the periods of the first and second oscillators. (See figure 6)

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (USPN 6,617,884).

With regards to claim 19, Wang et al. (USPN 6,617,884) teaches a method of measuring clock skew on a programmable logic device, the programmable logic device including a clock-distribution network having a source node connected to first, second, and third destination branches, and first, second, and third programmable logic blocks programmably connectable to the respective first, second, and third destination branches, each of the programmable logic blocks having an input terminal and an output terminal, the method comprising:

a. programming the programmable logic device to include a first ring oscillator (Col.7 lines 1-5) in which the first destination branch is connected to the input terminal of the first logic block and the output terminal of the first logic block is connected to the input terminal of the second logic block; (see figure 2 & 3) and
b. programming the programmable logic device to include a second ring oscillator (Col.7 lines 1-5) in which the third destination :branch is connected to the input terminal of the third logic block and the output terminal of the third logic block is connected to the input terminal of the second logic block. (see figure 2 & 3)

With regards to claim 20, Wang et al. (USPN 6,617,884) teaches the input terminal of the second logic block is a synchronous input terminal. (Col.1, lines 18-45)

With regards to claim 21, Wang et al. (USPN 6,617,884) teaches the first, second, and third logic blocks are arranged on the programmable logic device in a column. (see figure 2 & 3)

With regards to claim 22, Wang et al. (USPN 6,617,884) teaches the second logic block is physically between the first and third logic blocks. (see figure 2 & 3)

With regards to claim 23, Wang et al. (USPN 6,617,884) teaches the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth programmable logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the programmable logic blocks having an input terminal and an output terminal, the method further comprising: c. programming the programmable logic device to include a third ring oscillator in which the fourth destination branch is connected to the input terminal of the fourth logic block and the output terminal of the fourth logic block is connected to the input terminal of the fifth logic block; and d. programming the programmable logic device to include a fourth ring oscillator in which the sixth destination branch is connected to the input terminal of the sixth logic block and the output terminal of the sixth logic block to the input terminal of the fifth logic block. (See figure 2)

With regards to claim 24, Wang et al. (USPN 6,617,884) teaches connecting the output terminal of the first logic block to the input terminal of the second logic block establishes a first net, connecting the output terminal of the second logic block to the input terminal of the second logic block establishes a second net, connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block establishes a third net, and connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block establishes a fourth net, the method further comprising defining the first and third nets to be identical and defining the second and fourth nets to be identical.(see figure 2)

With regards to claim 25, Wang et al. (USPN 6,617,884) teaches configuring the programmable logic device to include the first and second delay elements in respective first and second oscillators. (Col.2, lines 16-35)

With regards to claim 26, Wang et al. (USPN 6,617,884) teaches comparing the periods of the first and second oscillators. (Col. 1, lines 50-55)

Claim Objections

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

In response to applicant's amendment, the recitation " a method of measuring signal skew on a programmable logic device, the logic device including a signal tree..." has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Response to Arguments

During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

In this instance the subject matter that is claimed can be broadly interpreted since claimed invention is recited in the preamble. Subject matter claimed in the preamble does not carry patentable weight. Therefore the claimed invention reads on the prior art of record.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wang et al. (USPN 6,642,758) teaches a voltage temperature and process independent programmable phase shift for PLL, Wang et al (USPN

6,369,624) teaches a programmable phase shift circuitry and Winegarden et al. (USPN 6,467,009) teaches a configurable processor system unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 703-308-0332. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Aditya S. Bhat
November 24, 2003

John Barlow
Supervisory Patent Examiner
Technology Center 2800